THAT WHICH IS CLAIMED IS:

1. Microprocessor comprising means for selecting an operating mode (M1) of the microprocessor, the selection means comprising:

- a counter (CNTR) having a counting input (E1) and a reset input (E2), and

- means (A2, I2) for coupling the counting input (E1) to a first terminal (P1) of the microprocessor, characterized in that the selection means further comprise:

- means (A1, I1) for coupling the reset input (E2) of the counter to a second terminal (P2) of the microprocessor, and

- means (R1), within or outside the microprocessor, for maintaining by default the reset input (E2) of the counter at a first logic value ("1") ensuring the maintaining at zero of the counter in the absence of a control signal (CS) likely to be applied to the second terminal (P2) for activating the counter.

2. Microprocessor according to claim 1, wherein the means for coupling the reset input (E2) of the counter to the second terminal (P2) of the microprocessor comprise a logic circuit (AI, I1) comprising an output coupled to the reset input (E2), a first input coupled to the second terminal (P2) of the microprocessor, and a second input receiving a signal (RESET) ensuring the inhibition of the output of the logic circuit (A1, I1) with regard to its first input outside selection periods of the operating mode of the microprocessor.

3. Microprocessor according to claim 2, wherein the inhibition signal of the logic circuit (A1, I1) is a reset signal (RESET) of the microprocessor.

4. Microprocessor according to claim 3, wherein the logic circuit comprises an AND-gate (A1) having a first input connected to the second terminal (P2) and a second input connected to the output of an inverting gate (I1) receiving as an input the reset signal (RESET) of the microprocessor.

5. Microprocessor according to one of the claims 1 to 4, wherein the means for maintaining by default the reset input (E2) of the counter at a first logic value ("1") comprise a bias resistor (R1).

6. Microprocessor according to one of the claims 1 to 5, wherein the output of the counter is applied to a central processing unit (CPU) of the microprocessor by means of a decoder (DEC) delivering, to the central processing unit, mode bits (M0, M1), the value of which depends on a counting result (N) delivered by the counter.

7. Microprocessor according to one of the claims 1 to 6, wherein the means for coupling the counting input (E1) of the counter to a first terminal (P1) of the microprocessor comprise a logic circuit (A2, I2) comprising an output coupled to the counting input (E1), a first input coupled to the first terminal (P1) of the microprocessor, and a second input receiving a signal (RESET) ensuring the inhibition of the output of the logic circuit (A2, I2) with regard to

its first input outside selection periods of the operating mode of the microprocessor.

8. Microprocessor according to one of the claims 1 to 7, wherein the operating mode (M1) is a test or a servicing mode requiring the application of a predetermined number (N1-N2) of electric pulses to the counting input (E1) of the counter during a selection period of the operating mode of the microprocessor.

9. Microprocessor according to one of the claims 1 to 8, wherein the first and the second terminals (P1, P2) as input/output ports of the microprocessor which are used as such outside selection periods of the operating mode of the microprocessor.

10. Method of selecting an operating mode (M1) of a microprocessor by means of a counter (CNTR) having a counting input (E1) and a reset input (E2), comprising a step of applying a predetermined number (N1-N2) of pulses (MS) to the counting input (E1) by means of a first terminal (P1) of the microprocessor, characterized in that it comprises the steps of:

- providing means (A1, I1) for coupling the reset input (E2) of the counter to a second terminal (P2) of the microprocessor,

- driving the reset input (E2) of the counter by means of a control signal (CS) applied to the second terminal (P2) of the microprocessor, so as to activate the counter, and

- providing means (R1), within or outside the microprocessor, for maintaining by default the reset input (E2) of the counter at a first logic value ("1")

ensuring the maintaining at zero of the counter in the absence of the control signal (CS).

11. Method according to claim 10, comprising a step of providing a first logic circuit (AI, I1) comprising an output coupled to the reset input (E2) of the counter, a first input coupled to the second terminal (P2) of the microprocessor, and a second input receiving a signal (RESET) ensuring the inhibition of the output of the logic circuit (A1, I1) with regard to its first input outside selection periods of the operating mode of the microprocessor.

12. Method according to one of the claims 10 and 11, comprising a step of providing a second logic circuit (A2, I2) comprising an output coupled to the counting input (E1) of the counter, a first input coupled to the first terminal (P1) of the microprocessor, and a second input receiving a signal (RESET) ensuring the inhibition of the output of the logic circuit (A2, I2) with regard to its first input outside selection periods of the operating mode of the microprocessor.

13. Method according to one of the claims 11 and 12, wherein the inhibition signal is a reset signal (RESET) of the microprocessor.

14. Method according to one of the claims 10 to 13, wherein the operating mode (M1) is a test or a servicing mode selected by applying a predetermined number (N1-N2) of electric pulses to the counting input

(E1) of the counter while a reset signal (RESET) of the microprocessor has an active value ("0").